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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,222	01/18/2002	Jinghui Lu	X-1055 US	7174

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,222	LU ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,19-23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *19-23* is/are allowed.

6)☒ Claim(s) *1-4,8-14 and 25-27* is/are rejected.

7)☒ Claim(s) *5-7,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The new Oath/Declaration was received on 06/24/2005. The new Oath/Declaration is accepted by the Examiner.

Drawings

The modifications to the drawings were received on 10/06/2005. These modifications are accepted by the Examiner.

Specification

The modifications to the specification were received on 10/06/2005. These modifications are accepted by the Examiner.

Response to Arguments

Regarding claim 1:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Shimamoto, however, provides an integrated circuit that includes only half of the conversion process to that claimed. In Shimamoto, data is first parallel-to-serial converted in integrated circuit block 7 of Fig. 2 and provided through a connector 3 to a different integrated circuit 19 having a second connector 15 shown in Fig. 3. Circuit 19 of Fig. 3 provides conversion from serial to parallel to send data to a display panel. Receiver compensation is provided in Fig. 3 in blocks 22-26, as noted by the Office Action, but no subsequent parallel to serial conversion occurs in this integrated circuit 19, as claimed in claim 1. Parallel data is simply sent to a display 17 in

Shimamoto. Accordingly, without Shimamoto describing an integrated transceiver with all the elements of claim 1, Applicants maintain that claim 1 is allowable as not anticipated by Shimamoto under 35 U.S.C. 102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto discloses an integrated high-speed parallel-to-serial and serial-to-parallel transceiver, where the transceiver comprises a receiver section that includes a receiver clocking circuit operably coupled to produce at least one high frequency receiver clock (figure 3 column 3 lines 1-56 and column 6 lines 15-67); serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency receiver clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); and receiver compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the receiver clocking circuit and the serial to parallel module (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); transmitter section that includes: transmitter clocking circuit operably coupled to produce at least one high frequency transmitter clock (figure 2 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency transmitter clock (figure 2 block 7 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); and transmitter compensation operable to at least partially compensate for at least one of the integrated circuit operational limitations and the integrated circuit fabrication limitations of at least

one of the transmitter clocking circuit and the parallel to serial module (figure 2 blocks 9-12 column 3 lines 1-56 and column 5 line 40 to column 6 line 14).

For these reasons and the reason stated in the previous Office action, the rejection of claim 1 is maintained.

Regarding claim 2:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Shimamoto, however, describes separation of a "parallel" input signal into even and odd "parallel" data. See col. 3, lines 2-8 of Shimamoto, indicating the data is converted to parallel" before separation. In contrast, the even/odd splitter of claim 1 recites separating "serial" data into odd and even serial data. Claim 2 is, thus believed allowable as not anticipated by Shimamoto under 35 U.S.C. 102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto also discloses that serial to parallel module and the receiver compensation further comprise an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data (figures 3 and 6 block 20 column 3 lines 1-56

and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37). The separation is produced before the conversion that is the reason why there are 2 blocks one foe the even (block 20) and one for the odd (block 19). For these reasons and the reason stated in the previous Office action, the rejection of claim 2 is maintained.

Regarding claim 4:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Regarding claim 4, the Office Action states that Shimamoto discloses use of "differential flip-flops" (fig. 7, col. 7 line 27 to col. 8 line 47). Shimamoto, however, only appears to show standard D-type flip-flops in Fig. not differential flip-flops. In contrast, Applicants' Fig. 2 shows flip-flops receiving differential clock signals (flip-flops each receiving two complementary clocks), as claimed in claim 4. Claim 4 is, thus, believed allowable as not anticipated by Shimamoto under 35 U.S.C. 102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47).

Figure 7 shows the flip-flops receiving two complementary clocks SHFCLK and SHFCLK# (see figure 8a and 8b). For these reasons and the reason stated in the previous Office action, the rejection of claim 4 is maintained.

Regarding claim 8:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Shimamoto do not show such a combining of odd/even data. The data remains separated and provided to connector 3 in Fig. 5. Data remains separated from the connector, as shown in Fig. 6 when it is converted back to serial in blocks 19 and 20. Accordingly, claim 8 is believed allowable as not anticipated by Shimamoto under 35 U.S.C. 102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto also discloses a combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data (figures 5 and 7 block 3 column 7 line 27 to column 8 line 57). The connector in figure 6 is element 15 and the connector in figure 5 is element 3, that how it is shown in figure 2 in this connector it is not difference between odd/even. For these reasons and the reason stated in the previous Office action, the rejection of claim 8 is maintained.

Regarding claim 9:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "neither of blocks 1 or 29 of figs. 5 and 7 of Shimamoto show a differential input interface, with both true and complementary signals. None appears to be described in col. 7 or col. 8 of Shimamoto. Further, col. 7 and col. 8 of Shimamoto do not disclose any calibration of the input impedance of the transmitter interface. Accordingly, claim 9 is believed allowable as not anticipated by Shimamoto under 35 U.S.C. 102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto discloses differential input interface having a calibrated input impedance (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57); and buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57). Figure 7 shows the flip-flops receiving two complementary clocks SHFCLK and SHFCLK# (see figure 8a and 8b). Block 39 is a driver used as a calibrated input impedance. For these reasons and the reason stated in the previous Office action, the rejection of claim 9 is maintained.

Regarding claim 10:

Applicant's arguments filed on 10/06/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Shimamoto, however, only appears to show and describe standard D-type flip flops in Fig. 7, not differential flip-flops. Claim 10 is, thus, believed allowable as not anticipated by Shimamoto under 35 U.S.C.102."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Shimamoto discloses each of the even and add parallel to serial converters further comprises a plurality of interoperably coupled high-speed, low power, differential flip flops (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57). Figure 7 shows the flip-flops receiving two complementary clocks SHFCLK and SHFCLK# (see figure 8a and 8b). For these reasons and the reason stated in the previous Office action, the rejection of claim 10 is maintained.

Regarding claims 21, 22, 23:

Because Applicant's arguments filed on 10/06/2005 are persuasive regarding claim 19, claims 21-23 are allowable.

Regarding claims 25 and 27:

See response to argument to claims 2 and 4 respectively.

Regarding claims 3 and 26.

The rejections are maintained because the rejections of claims 1 and 25 are maintained.

Regarding claim 11:

The rejection are maintained because the rejection of claim 1 is maintained.

Regarding claim 5:

Applicant's arguments filed on 10/06/2005 have been fully considered and they are persuasive.

Regarding claims 19 and 28:

Applicant's arguments filed on 10/06/2005 have been fully considered and they are persuasive.

Regarding claims 13 and 14:

The rejections are maintained because the rejection of claims 1 is maintained.

Regarding claims 20 and 29:

Because Applicant's arguments filed on 10/06/2005 are persuasive regarding claims 19 and 28, claims 20 and 29 are allowable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 8-10, 25 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimamoto (US 6147672).

As per claim 1 Shimamoto discloses an integrated high-speed parallel-to-serial and serial-to-parallel transceiver, where the transceiver comprises a receiver section that includes a receiver clocking circuit operably coupled to produce at least one high frequency receiver clock (figure 3 column 3 lines 1-56 and column 6 lines 15-67); serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency receiver clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); and receiver compensation operable to at least partially compensate for at least one of integrated circuit operational

limitations and integrated circuit fabrication limitations of at least one of the receiver clocking circuit and the serial to parallel module (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); transmitter section that includes: transmitter clocking circuit operably coupled to produce at least one high frequency transmitter clock (figure 2 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency transmitter clock (figure 2 block 7 column 3 lines 1-56 and column 5 line 40 to column 6 line 14); and transmitter compensation operable to at least partially compensate for at least one of the integrated circuit operational limitations and the integrated circuit fabrication limitations of at least one of the transmitter clocking circuit and the parallel to serial module (figure 2 blocks 9-12 column 3 lines 1-56 and column 5 line 40 to column 6 line 14).

As per claim 2 Shimamoto discloses claim 1. Shimamoto also discloses that serial to parallel module and the receiver compensation further comprise an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data (figures 3 and 6 block 20 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel

odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37).

As per claim 4 Shimamoto discloses claim 2. Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47).

As per claim 8 Shimamoto discloses claim 1. Shimamoto also discloses an interface operably coupled to receive the outbound parallel data (figures 5 and 7 block 1 column 7 line 27 to column 8 line 57); even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data (figures 5 and 7 block 6 column 7 line 27 to column 8 line 57); odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into odd serial outbound data (figures 5 and 7 block 5 column 7 line 27 to column 8 line 57); combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data (figures 5 and 7 block 3 column 7 line 27 to column 8 line 57); and driver operably coupled to produce the outbound serial data from the combined serial data (figures 5 and 7 blocks 61, 33, 35, 41 column 7 line 27 to column 8 line 57).

As per claim 9 Shimamoto discloses claim 8. Shimamoto also discloses differential input interface having a calibrated input impedance (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57); and buffer operably coupled to temporarily

store the outbound parallel data received via the differential input interface (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 10 Shimamoto discloses claim 8. Shimamoto also discloses each of the even and add parallel to serial converters further comprises a plurality of interoperably coupled high-speed, low power, differential flip flops (figures 5 and 7 blocks 1 and 29 column 7 line 27 to column 8 line 57).

As per claim 25 Shimamoto discloses an integrated high-speed where the receiver comprises clocking circuit operably coupled to produce at least one high frequency clock (figure 3 block 21 column 3 lines 1-56 and column 6 lines 15-67); serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency clock (figure 3 block 20 column 3 lines 1-56 and column 6 lines 15-67); and compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the clocking circuit and the serial to parallel module (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); the serial to parallel module and the receiver compensation further comprise an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data (figure 3 blocks 22-26 column 3 lines 1-56 and column 6 lines 15-67); even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data (figures 3 and 6 block 15 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); even serial to parallel converter operably coupled to convert the serial even data into parallel even data

(figures 3 and 6 block 20 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data (figures 3 and 6 block 19 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37); and output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data (figures 3 and 6 block 17 column 3 lines 1-56 and column 6 lines 15-67 and column 7 lines 27-37).

As per claim 27 Shimamoto discloses claim 25. Shimamoto also discloses the use of a plurality of interoperably coupled high-speed, low power, differential flip flops (figure 7 column 7 line 27 to column 8 line 47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) as applied to claim 2 above, and further in view of Ipek (US 20010018334).

As per claim 3 Shimamoto discloses claim 2. Shimamoto also discloses an interface and an amplifier (figure 3 blocks 15 and 22-26 column 3 lines 1-56 and column 5 line 40 to column 6 line 14). Shimamoto doesn't disclose an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier. Ipek discloses an inductive amplifier operably coupled to the

interface and a feed forward boost module operably coupled to the inductive amplifier (figure 1 paragraphs [0013] to [0025]). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 3.

As per claim 26 Shimamoto discloses claim 25. Shimamoto also discloses an interface and an amplifier (figure 3 blocks 15 and 22-26 column 3 lines 1-56 and column 5 line 40 to column 6 line 14). Shimamoto doesn't disclose an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier. Ipek discloses an inductive amplifier operably coupled to the interface and a feed forward boost module operably coupled to the inductive amplifier (figure 1 paragraphs [0013] to [0025]). Shimamoto and Ipek are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto boosted inductive amplifier disclosed by Ipek. The suggestion/motivation for doing so would have been to design a receiver with a large dynamic range and a high linearity, and having a low noise (Ipek abstract). Therefore, it

would have been obvious to combine Shimamoto with Ipek to obtain the invention as specified in claim 26.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) as applied to claim 1 above, and further in view of Welland (US 6167245). Shimamoto discloses claim 1. Shimamoto doesn't disclose a phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the at Least one high frequency transmitter clock; charge pump operably coupled to produce a voltage representative of the difference signal; filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation; voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation; post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock; and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock. Welland discloses phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference lock and a feedback clock that is representative of the at Least one high frequency transmitter clock (figure 1-6 block 402 column 5 line 54 to column 12 line 18); charge pump operably coupled to produce a voltage representative of the difference signal (figure 1-6 block 402 column 5 line 54 to column 12 line 18); filter operably coupled filter the voltage representation of the difference signal to produce a filtered difference representation (figure 1-6 block 210 column 5 line 54 to column 12 line 18); voltage

controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation (figure 1-6 block 400 column 5 line 54 to column 12 line 18); post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock (figure 1-6 block 624 column 5 line 54 to column 12 line 18); and divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock (figure 1-6 block 406 column 5 line 54 to column 12 line 18). Shimamoto and Welland are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto with the High frequency PLL disclosed by Welland. The suggestion/motivation for doing so would have been synthesizing high-frequency signals with low phase noise and other impurity requirements (Welland abstract). Therefore, it would have been obvious to combine Shimamoto with Welland to obtain the invention as specified in claim 11.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) in view of Welland (US 6167245) as applied to claim 11 above, and further in view of Kim (US 20010030562).

As per claim 13 Shimamoto and Welland discloses claim 11. Shimamoto and Welland don't disclose a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock. Kim discloses a duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock (figure 8 paragraphs [0043] to [0046]. Shimamoto, Welland

and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 13.

As per claim 14 Shimamoto, Welland and Kim discloses claim 13. Welland also discloses a phase error correction circuit operably coupled to correct phase error of the at least one high frequency transmitter clock (figure 1-6 block 206 column 5 line 54 to column 12 line 18). Shimamoto, Welland and Kim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the duty cycle distortion correction disclosed by Kim. The suggestion/motivation for doing so would have been to avoid duty cycle errors (Kim paragraph [004]). Therefore, it would have been obvious to combine Shimamoto and Welland with Kim to obtain the invention as specified in claim 14.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (US 6147672) in view of Welland (US 6167245) as applied to claim 11 above, and further in view of Mohindra (US 6148047). Shimamoto and Welland disclose claim 11. Shimamoto and Welland don't disclose an offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation.

Mohindra discloses offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation (figure 8 column 6 lines 8-61). Shimamoto, Welland and Mohindra are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in the transceiver circuit disclosed by Shimamoto and Welland with the DC offset compensation disclosed by Mohindra. The suggestion/motivation for doing so would have been to reduce distortion of the signal (Mohindra column 1 lines 36-42). Therefore, it would have been obvious to combine Shimamoto and Welland with Mohindra to obtain the invention as specified in claim 12.

Allowable Subject Matter

Claims 19-23 are allowed.

Claims 5-7 and 28-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: claims 5-7, 19-23 and 28-29 are allowed because the references cited fail to teach, as applicant has, a fine phase detector coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock; fine charge pump operably coupled to produce a voltage representative of the fine difference signal; coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock

that is representative of the at least one high frequency receiver clock; and a coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
10-25-2005

KEVIN BURD
PRIMARY EXAMINER